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(71) Applicant: **FUJITSU LIMITED**
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211 (JP)

(71) Applicant: **FUJITSU VLSI LIMITED**
1844-2, Kozoji-cho 2-chome
Kasugai-shi Aichi 487 (JP)

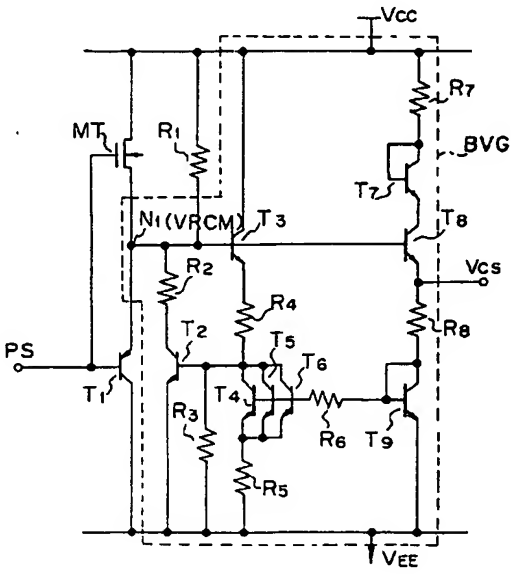
(72) Inventor: **Nonaka, Kazuyuki, c/o Fujitsu VLSI Limited**
1844-2, Kozoji-cho 2-chome
Kasugai-shi, Aichi 487 (JP)
Inventor: **Aisaka, Tetsuya, c/o Fujitsu VLSI Limited**
1844-2, Kozoji-cho 2-chome
Kasugai-shi, Aichi 487 (JP)

(74) Representative: **Gibbs, Christopher Stephen et al**
Haseltine Lake & Co. Hazlitt House 28 Southampton Buildings
Chancery Lane, London WC2A 1AT (GB)

(54) Bias voltage generation circuit of ECL level for decreasing power consumption thereof.

(57) A bias voltage generation circuit comprises a bias voltage generation portion (BVG) having a bias control node (N_1), a first switching unit (T_1), and a second switching unit (MT, MTP). The bias voltage generation portion (BVG) is used to generate a bias voltage (Vcs) of a predetermined potential and supply the bias voltage (Vcs) to an ECL circuit during an operation period (t_0), and the first switching unit (T_1) is used to drop the bias voltage (Vcs) during a standby period (t_1) in response to a bias voltage control signal (PS). The second switching unit (MT, MTP) is used to switch OFF during the standby period (t_1) to cut off a current flow through the bias control node (N_1) and switch ON during the operation period (t_0) to supply a current through the bias control node (N_1) in response to the bias voltage control signal (PS). Consequently, current flow during the standby period (t_1) can be reduced, and power consumption of the bias voltage generation circuit during the standby period (t_1) is minimal.

Fig. 2



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The present invention relates to a bias voltage generation circuit, more particularly, to a bias voltage generation circuit of an emitter coupled logic (ECL) level.

Conventionally, high-speed LSIs are constituted by emitter coupled logic (ECL) circuits, but the ECL circuits require large amounts of power. In recent years, high-speed LSIs of low power consumption have been required to realize a battery backup system, and various techniques have been developed and proposed to meet the requirement.

Note, one effective technique applying to ECL circuits is to make a standby state by dropping the bias voltage of the ECL circuits during a non-operation period, thereby saving on total power consumption during operation and non-operation periods. This technique externally controls the bias voltage of the ECL circuits generated by a bias voltage generation circuit. Further, the bias voltage generation circuit is also required to be of low power consumption by itself.

An object of the present invention is to provide a bias voltage generation circuit having small consumption power during a standby period. Namely, an object of the present invention is to reduce current flow to a negligible amount (less than about 10 microamperes: μ A) during a standby period.

According to the present invention, there is provided a bias voltage generation circuit comprising: a first power supply line; a second power supply line; a bias voltage generation portion having a bias control node, connected between the first power supply line and the second power supply line, for generating a bias voltage of a predetermined potential and supplying the bias voltage to a circuit during an operation period; a first switching unit, connected between the bias control node of the bias voltage generation portion and the second power supply line, for dropping the bias voltage during a standby period in accordance with a bias voltage control signal; and a second switching unit, connected between the bias control node and the first power supply line, for switching OFF during the standby period to cut off current flowing through the bias control node and switching ON during the operation period to supply a current through the bias control node in accordance with the bias voltage control signal.

The first switching unit may be constituted by a PNP-type bipolar transistor having base, collector and emitter electrodes, the base electrode receiving the bias voltage control signal, the collector electrode being connected to the second power supply line, and the emitter electrode being connected to the bias control node.

The second switching unit may be constituted by an N-type MIS transistor, a gate electrode of the N-type MIS transistor receiving the bias voltage control signal, The second switching unit may be constituted by a P-type MIS transistor, a gate electrode of the P-type MIS transistor receiving an inverted signal of the bias voltage control signal through an inverter. The ON-resistance value of the MIS transistor may correspond to a resistance value determined by the bias voltage generation portion. The MIS transistor may be constituted as a long-gate MIS transistor.

The bias voltage generation portion may include a compensation bipolar transistor, connected to the second power supply line and a resistor (R_2) connected between the bias control node and the compensation bipolar transistor, for compensating the bias voltage at the predetermined potential. The second switching unit may be switched OFF during the standby period to cut off the current flowing through the compensation bipolar transistor.

The bias voltage generation circuit may further comprise a resistor connected between the first power supply line and the bias control node in series to the second switching unit, the resistance value of the resistor corresponding to a resistance value determined by the bias voltage generation portion, the second switching unit being mainly used for a switching purpose, and the resistor being mainly used for providing a required resistance value. The bias voltage generation circuit may further comprise a pull-up resistor having a high resistance value, connected between the first power supply line and the bias control node. The first power supply line may be a high-potential power supply line, and the second power supply line may be a low-potential power supply line. The bias voltage generated by the bias voltage generation circuit may be supplied to an emitter coupled logic circuit during the operation period.

The present invention will be more clearly understood from the description of the preferred embodiments as set forth below with reference to the accompanying drawings, wherein:

Figure 1 is a circuit diagram showing an example of a bias voltage generation circuit according to the related art;

Figure 2 is a circuit diagram showing a first embodiment of a bias voltage generation circuit according to the present invention;

Figure 3 is a circuit diagram showing an ECL circuit to which the bias voltage generation circuit of the present invention is applicable;

Figure 4 is a block diagram showing an example of radio telephone equipment using the bias voltage generation circuit of the present invention;

Figure 5 is a circuit block diagram showing the prescaler shown in Fig. 4;

Figures 6A to 6C are timing charts for explaining an operation of the prescaler of Fig. 5;

Figure 7 is a circuit diagram showing a second embodiment of the bias voltage generation circuit according to the present invention; and

Figure 8 is a circuit diagram showing a third embodiment of the bias voltage generation circuit

according to the present invention.

For a better understanding of the preferred embodiments, the problems of the related art will be explained, with reference to Fig. 1.

Figure 1 shows an example of a bias voltage generation circuit according to the related art. As shown in Fig. 1, the bias voltage generation circuit comprises a PNP-type bipolar transistor T_{101}, a plurality of NPN-type bipolar transistors T_{102} to T_{109}, and a plurality of resistors R_{101} to R_{108} . The transistor T_{101} has a base electrode connected to a bias voltage control signal input terminal (PS), an emitter electrode, which is a node n_1 and generally called as VRCM, connected to a high-potential power source (first power supply line) V_{CC} through the resistor R_{101}, and a collector electrode connected to a low-potential power source (second power supply line) V_{EE}. The transistor T_{102} has a collector electrode connected, through the resistor R_{102}, to the emitter electrode (node n_1) of the transistor T_{101} as well as to the base electrodes of the transistors T_{103} and T_{108}, an emitter electrode connected to the low-potential power source V_{EE}, and a base electrode connected to the collector electrodes of the transistors T_{104}, T_{105}, and T_{106} as well as to the low-potential power source V_{EE} through the resistor R_{103}. The transistor T_{103} has a collector electrode connected to the high-potential power source V_{CC}, and an emitter electrode connected to the base electrode of the transistor T_{102} through the resistor R_{104}.

The base electrodes of the transistors T_{104}, T_{105}, and T_{106} are connected to one another and commonly to the collector and base electrodes of the transistor T_{109} through the resistor R_{106}, and the emitter electrodes thereof are connected to one another and to the low-potential power source V_{EE} through the resistor R_{105}. The collector electrode of the transistor T_{107} is connected to its base electrode as well as to the high-potential power source V_{CC} through the resistor R_{107}, and the emitter electrode thereof is connected to the collector electrode of the transistor T_{108}. The emitter electrode of the transistor T_{106} is connected to a bias voltage output terminal Vcs as well as to the collector electrode of the transistor T_{109} through the resistor R_{108}. The emitter electrode of the transistor T_{109} is connected to the low-potential power source V_{EE}.

Note, the transistors T_{104}, T_{105}, T_{106}, and T_{109} are the same size, and these transistors (T_{104}, T_{105}, T_{106}, T_{109}) are used to compensate for the temperature dependency thereof. Further, the transistor T_{102} is used to compensate for the bias voltage Vcs at the predetermined potential (-4.0, or 1.2 volts). In addition, as shown in Fig. 1, a bias voltage generation portion BVG' is constituted by the bipolar transistors T_{102} to T_{109}, and the resistors R_{101} to R_{108}.

In the above bias voltage generation circuit shown in Fig. 1, for example, a potential of the high-potential power source V_{CC} is defined to be 0 (or 5.2) volts, a potential of the low-potential power source V_{EE} is defined to be -5.2 (or 0) volts, and the bias voltage Vcs is defined to be -4.0 (or 1.2) volts. Further, for example, each resistance value of the resistor R_{101} and the resistor R_{105} is defined to be 20 kΩ.

In the bias voltage generation circuit of Fig. 1. the bias voltage control signal PS supplied to the bias voltage control signal input terminal (PS) is dropped during a standby period (corresponding to a period t_1 shown in Fig. 6B) to turn ON the PNP-type bipolar transistor T_{101}. Therefore, a level at the node n_1 (VRCM) is dropped to decrease an output voltage (bias voltage) Vsc. As a result, power consumption of an ECL circuit to which the bias voltage is supplied is reduced during the standby period.

As described above, the bias voltage generation circuit shown in Fig. 1 turns ON the transistor T_{101} during a standby period to drop a level at the node n_1, thereby dropping the output voltage Vcs. The resistance value of the resistor R_{101} must not be too high because it supplies a collector current to the transistor T_{102} during operation. This means that a current flowing to the resistor R_{101} (which is defined to be about several tens kiloohms) may remain as an emitter current to the transistor T_{101} during a standby period. The current flowing to the resistor R_{101} is, for example, about 100 μ A, although it depends on a circuit constant. This will be a big problem to be solved, in particular, for radio telephone equipment using a battery backup system.

Below, the preferred embodiments of a bias voltage generation circuit according to the present invention will be explained, with reference to the accompanying drawings.

Figure 2 is a circuit diagram showing a first embodiment of a bias voltage generation circuit according to the present invention. As shown in Fig. 2, the bias voltage generation circuit of the first embodiment comprises an N-type MIS transistor MT, a PNP-type bipolar transistor T_1, a plurality of NPN-type bipolar transistors T_2 to T_9, and a plurality of resistors R_1 to R_8.

The transistor T_1 has a base, collector and emitter electrodes. The base electrode of the transistor T_1 is connected to a bias voltage control signal input terminal (PS) as well as to the gate electrode of the MIS transistor MT, the emitter electrode thereof, which is a node n_1 and generally called as VRCM, is connected to the drain electrode of the transistor MT, and the collector electrode thereof is connected to a low-potential power source (second power supply line) V_{EE}. The source electrode of the transistor MT is connected to a high-potential power source (first power supply line) V_{CC}.

The collector electrode of the transistor T_2 is connected to the emitter electrode (node N_1) of the transistor T_1 through the resistor R_2. The node N_1 (VRCM) is connected to the high-potential power source V_{CC}

through the resistor R_1 as well as to the base electrodes of the transistors T_3 and T_8. The emitter electrode of the transistor T_2 is connected to the low-potential power source V_{EE}, and the base electrode thereof is connected to the collector electrodes of the transistors T_4, T_5, and T_6 as well as to the low-potential power source V_{EE} through the resistor R_3. The collector electrode of the transistor T_3 is connected to the high-potential power source V_{CC}, and the emitter electrode thereof is connected to the base electrode of the transistor T_2 through the resistor R_4.

The base electrodes of the transistors T_4, T_5, and T_6 are connected to one another and commonly to the collector and base electrodes of the transistor T_9 through the resistor R_6, and the emitter electrodes thereof are connected to one another and to the low-potential power source V_{EE} through the resistor R_5. The collector electrode of the transistor T_7 is connected to its base electrode as well as to the high-potential power source V_{CC} through the resistor R_7, and the emitter electrode thereof is connected to the collector electrode of the transistor T_8. The emitter electrode of the transistor T_8 is connected to the bias voltage output terminal (Vcs) as well as to the collector electrode of the transistor T_9 through the resistor R_8. The emitter electrode of the transistor T_9 is connected to the low-potential power source V_{EE}.

Note, the transistors T_4, T_5, T_6, and T_9 are the same size, and these transistors (T_4, T_5, T_6; T_9) are used to compensate for the temperature dependency thereof. Further, the transistor T_2 is used to compensate for the bias voltage Vcs at the predetermined potential (-4.0, or 1.2 volts). Namely, the transistor T_2 compensates for temperature dependency of the bias voltage Vcs. Further, as shown in Fig. 2, a bias voltage generation portion BVG is constituted by the bipolar transistors T_2 to T_9, and the resistors R_2 to R_8.

In the above bias voltage generation circuit shown in Fig. 2, for example, a potential of the high-potential power source V_{CC} is defined to be 0 (or 5.2) volts, a potential of the low-potential power source V_{EE} is defined to be -5.2 (or 0) volts, and the bias voltage Vcs is defined to be -4.0 (or 1.2) volts. Further, for example, the resistance value of the resistor R_5 is defined to be 20 kΩ , and the ON-resistance value of the MIS transistor MT is defined to be 20 kΩ . Note, the ON-resistance value of the MIS transistor MT corresponds to that of the resistor R_{101} shown in Fig. 1,

Next, the operation of the bias voltage generation circuit of Fig. 2 will be explained.

During a standby period (corresponding to a period t_1 shown in Fig. 6B) of the bias voltage generation circuit of this embodiment shown in Fig. 2, the bias voltage control signal PS supplied to the bias voltage control signal input terminal (PS) is dropped to turn ON the PNP-type bipolar transistor T_1. Therefore, a level at the node N_1 falls to set the output voltage (bias voltage) Vcs to a low potential. Note, at this time, the bias voltage control signal PS is also supplied to the gate of the N-type MIS transistor MT, so that the transistor MT is turned OFF by the bias voltage control signal PS. Consequently, almost no current flows through the turned OFF transistor MT and the node N_1 during the standby period. In this way, power consumption of an ECL circuit to which the bias voltage is supplied is saved during the standby period. Further, power consumption of the bias voltage generation circuit is also reduced by cutting OFF the current flowing through the MIS transistor MT and the node N_1.

During an operation period (corresponding to a period to shown in Fig. 6B) in which the bias voltage generation circuit of this embodiment generates a bias voltage of predetermined level, the bias voltage control signal PS supplied to the gate of the N-type MIS transistor MT rises to turn ON the transistor MT. Because of the ON-resistance (for example, several tens kiloohms) of the transistor MT, the transistor functions similar to the resistor R_{101} of Fig. 1. Namely, during operation, the ON-resistance of the transistor MT works to supply a collector current to the bipolar transistor T_2 for providing the bias voltage Vcs of predetermined potential. According to the bias voltage generation circuit of Fig. 2, the gate length of the N-type MIS transistor MT is long enough to provide the ON-resistance of, for example, several kiloohms. The resistor R_1 of Fig. 2 is a pull-up resistor, which supplies a very weak collector current to the transistor T_1. The resistor R_1 may have a high resistance value of about several megaohms. Accordingly, a current of several microamperes will flow through the pull-up resistor R_1, which causes no problem with power consumption in actual use.

Figure 3 is a circuit diagram showing an ECL circuit to which the bias voltage generation circuit of the present invention is applicable, and the ECL circuit is a basic one. As shown in Fig. 3, the ECL circuit comprises transistors T_{31} to T_{37} and resistors R_{31} to R_{35}.

The output (bias voltage) Vcs of the bias voltage generation circuit of the invention is supplied to various ECL circuits. As shown in Fig. 3, for example, the bias voltage Vcs is applied to base electrodes of the transistors T_{35}, T_{36}, and T_{37} of the ECL circuit, and during a standby period, the bias voltage generation circuit drops the bias voltage Vcs to reduce power consumption in the ECL circuit. Note, the bias voltage generation circuit is applicable for providing a bias voltage to the basic ECL circuit of Fig. 3 as well as other circuits.

Figure 4 is a block diagram showing an example of radio telephone equipment using the bias voltage generation circuit of the present invention.

As shown in Fig. 4, the radio telephone equipment, which is generally provided with a battery backup system, comprises a microprocessor unit (MPU) 1, a PLL control circuit 2, a prescaler 3, a phase

comparator 4, a charge pump circuit 5, a low pass filter (LPF) 7, a voltage controlled oscillator (VCO) 6, and a crystal oscillator 11. Note, as shown in Fig. 4, the bias voltage generation circuit of the present invention is included in the prescaler 3, and a power save signal (bias voltage control signal) PS is supplied to the bias voltage generation circuit. Further, as shown in Fig. 4, a radio frequency RF (RF_{out}, RF_{in}) generated by the VCO 6 is returned to the PLL control circuit 2 through the prescaler 3.

Figure 5 is a circuit block diagram showing the prescaler shown in Fig. 4.

As shown in Fig. 5, the prescaler 3 comprises a bias voltage generation circuit 30, four T-type flip-flops 31 to 34, and inverters 35 and 36. Note, the flip-flops 31 to 34 are connected in series, the radio frequency RF_{in} output from the VCO 6 is supplied to the flip-flop 31, and the signal f_{out} output from the flip-flop 34 is supplied to the PLL control circuit 2. Further, the flip-flops 31 to 34 are constituted by ECL circuits to realize a high-speed operation.

The power save signal (bias voltage control signal) PS output from the MPU 1 is supplied to the bias voltage generation circuit 30 through the inverters 35 and 36, and the bias voltage Vcs output from the bias voltage generation circuit 30 is applied to the flip-flops 31 to 34. Note, the bias voltage generation circuit 30 is not only applied to the prescaler 3 of the radio telephone equipment, but the bias voltage generation circuit 30 can also be applied to various ECL circuits.

Figures 6A to 6C are timing charts for explaining an operation of the prescaler of Fig. 5.

As shown in Fig. 6A, the power save signal (bias voltage control signal) PS is changed to a high level during 100 milliseconds (msec.) by 1 second (sec.). Namely, one period of the power save signal PS is determined to be 1 sec., and the power save signal PS is at a high level during 100 msec. and at a low level during 900 msec. in each period thereof.

In Fig. 6B, a reference t_0 denotes an operation period corresponding to the period that the power save signal PS is at a high level, and a reference t_1 denotes a standby period corresponding to the period that the power save signal PS is at a low level. Further, a reference P_{01} denotes a timing of starting the operation of the prescaler 3, and a reference P_{02} denotes a timing of stopping the operation of the prescaler 3.

Namely, as shown in Figs. 2, 6A to 6C, during the standby period t_1, the power save signal PS is dropped to turn ON the PNP-type bipolar transistor T_1, and a level at the node N_1 falls to set the output voltage (bias voltage) Vcs to a low potential (-5.2, or 0 volts). Note, at this time, the power save signal PS is also supplied to the gate of the N-type MIS transistor MT, so that the transistor MT is turned OFF by the power save signal PS. Consequently, as shown in Fig. 6C, almost no current CC_1 (2 ~ 5 μ A) is used by the prescaler 3 during the standby period t_1.

On the other hand, during an operation period t_0, the power save signal PS rises to turn OFF the PNP-type bipolar transistor T_1, and a bias voltage Vcs is returned to a predetermined level (-4.0, or 1.2 volts). Further, the N-type MIS transistor MT is turned ON, and the ON-resistance of the transistor MT is provided between the high-potential power source V_{CC} and the node N_1, so that a collector current of the bipolar transistor T_2 for providing the bias voltage Vcs of predetermined potential starts to flow. Consequently, as shown in Fig. 6C, a current CC_0 (several tens mA) is used by the prescaler 3 during the operation period t_0.

Note, in Fig. 6C, a reference CC_{01} denotes a consumption current of the related art prescaler using the bias voltage generation circuit shown in Fig. 1 during the standby period t_1. Therefore, by applying the bias voltage generation circuit of the present invention, the consumption current of the prescaler 3 can be reduced from the current CC_{01} (several hundreds μ A) to the current CC_1 (2 ~ 5 μ A), during the standby period t_1.

Figure 7 is a circuit diagram showing a second embodiment of the bias voltage generation circuit according to the present invention.

By comparing the bias voltage generation circuit shown in Fig. 7 with that shown in Fig. 2, the bias voltage generation circuit shown in Fig. 7 further comprises a resistor R_0. The resistor R_0 is connected between the N-type MIS transistor MT and the node N_1. Note, other parts of this second embodiment are the same as those of the first embodiment of the bias voltage generation circuit shown in Fig. 2.

Note, the ON-resistance of a standard N-type MIS transistor is small, for example, several ohms. Accordingly, the transistor MT is used mainly for switching purposes, and the resistor R_0 mainly determines a resistance value (for example, several tens kiloohms) while the transistor MT is being ON. In Fig. 7, the resistor R_0 is disposed between the drain of the transistor MT and the node N_1, but the resistor R_0 may be disposed between the high-potential power source V_{CC} and the source of the transistor MT. For example, the ON-resistance value of the transistor MT is determined to be 1 kΩ (or 100 Ω), and the resistance value of the resistor R_0 is determined to be 19 kΩ (or 19.9 k Ω). In this case, when fluctuating the resistance value of the ON-resistance value of the transistor MT, the total resistance value is mainly due to that of the resistor R_0, and thus the manufacturing variation of the transistor MT does not influence to the bias voltage Vcs. Further, as shown in Fig. 7, in this second embodiment, the pull-up resistor R_1 is connected parallel with the series-connected MIS transistor MT and resistor R_0.

Figure 8 is a circuit diagram showing a third embodiment of the bias voltage generation circuit according to the present invention. As shown in Fig. 8, a P-type MIS transistor MTP can be used instead

of the N-type MIS transistor MT of Fig. 7. The gate of the P-type MIS transistor MTP receives an inverted signal of the bias voltage control signal PS through an inverter INV.

As described above, in a bias voltage generation circuit according to the present invention, a bias voltage generation circuit generates a bias voltage Vcs of predetermined potential during an operation period and drops the bias voltage during a standby period in response to a bias voltage control signal PS to save power consumption of the ECL circuit to which the bias voltage is supplied. The bias voltage generation circuit comprises a MIS transistor MT (MTP) to be switched ON and OFF in response to the bias voltage control signal. The MIS transistor MT (MTP) is switched OFF during the standby period to cut off current flow and ON during the operation period to supply a current to a bipolar transistor T_2 for providing the bias voltage of the predetermined potential.

In the bias voltage generation circuit of the present invention, the MIS transistor MT (MTP) is switched ON and OFF in response to the bias voltage control signal PS. During a standby period, the MIS transistor MT (MTP) is turned OFF to cut off a current, and during an operation period, the MIS transistor MT (MTP) is turned ON to supply a current to the bipolar transistor T_2 for providing the bias voltage of the predetermined potential.

As explained above, the bias voltage generation circuits according to the embodiments can reduce a current in the bias voltage generation circuits themselves during a standby period. In particular, the embodiments realize an elongated use with low power consumption required for battery driven communications equipment, etc.

Namely, in accordance with a bias voltage generation circuit of the present invention, the bias voltage generation circuit comprises a MIS transistor to be switched ON and OFF in response to a bias voltage control signal, and current flow is reduced to a negligible amount (less than about 10 μ A) during a standby period.

Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.

Claims

1. A bias voltage generation circuit including a first power supply line (V_{CC}), a second power supply line (V_{EE}), and a bias voltage generation portion (BVG) having a bias control node (N_1), connected between said first power supply line (V_{CC}) and said second power supply line (V_{EE}), for generating a bias voltage (Vcs) of a predetermined potential and supplying said bias voltage (Vcs) to a circuit during an operation period (t_0), characterized in that said bias voltage generation circuit comprises:

   a first switching means (T_1), connected between said bias control node (N_1) of said bias voltage generation portion (BVG) and said second power supply line (V_{EE}), for dropping said bias voltage (Vcs) during a standby period (T_1) in accordance with a bias voltage control signal (PS); and

   a second switching means (MT, MTP), connected between said bias control node (N_1) and said first power supply line (V_{CC}), for switching OFF during said standby period (t_1) to cut off current flowing through said bias control node (N_1) and switching ON during said operation period (t_0) to supply a current through said bias control node (N_1) in accordance with said bias voltage control signal (PS).

2. A bias voltage generation circuit according to claim 1, wherein said first switching means (T_1) is constituted by a PNP-type bipolar transistor having base, collector and emitter electrodes, said base electrode receiving said bias voltage control signal (PS), said collector electrode being connected to said second power supply line (V_{EE}), and said emitter electrode being connected to said bias control node (N_1).

3. A bias voltage generation circuit according to claim 1, wherein said second switching means (MT) is constituted by an N-type MIS transistor, a gate electrode of said N-type MIS transistor (MT) receiving said bias voltage control signal (PS).

4. A bias voltage generation circuit according to claim 1, wherein said second switching means (MTP) is constituted by a P-type MIS transistor, a gate electrode of said P-type MIS transistor (MTP) receiving an inverted signal of said bias voltage control signal (PS) through an inverter (INV).

5. A bias voltage generation circuit according to claim 3 or 4, wherein the ON-resistance value of said MIS transistor (MT, MTP) corresponds to a resistance value determined by said bias voltage generation portion (BVG).

6. A bias voltage generation circuit according to claim 5, wherein said MIS transistor (MT, MTP) is constituted as a long-gate MIS transistor.

7. A bias voltage generation circuit according to any one of the preceding claims, wherein said bias

voltage generation portion (BVG) includes a compensation bipolar transistor (T_2), connected to said second power supply line (V_{EE}) and a resistor (R_2) connected between said bias control node (N_1) and said compensation bipolar transistor (T_2), for compensating said bias voltage (Vcs) at said predetermined potential.

8. A bias voltage generation circuit according to claim 7, wherein said second switching means (MT, MTP) is switched OFF during said standby period (t_1) to cut off the current flowing through said compensation bipolar transistor (T_2).

9. A bias voltage generation circuit according to any one of the preceding claims, wherein said bias voltage generation circuit further comprises a resistor (R_0) connected between said first power supply line (V_{CC}) and said bias control node (N_1) in series to said second switching means (MT, MTP), the resistance value of said resistor (R_0) corresponding to a resistance value determined by said bias voltage generation portion (BVG), said second switching means (MT, MTP) being used mainly for a switching purpose, and said resistor (R_0) being used mainly for providing a required resistance value.

10. A bias voltage generation circuit according to any one of the preceding claims, wherein said bias voltage generation circuit further comprises a pull-up resistor (R_1) having a high resistance value, connected between said first power supply line (V_{CC}) and said bias control node (N_1).

11. A bias voltage generation circuit according to any one of the preceding claims, wherein said first power supply line (V_{CC}) is a high-potential power supply line, and said second power supply line (V_{EE}) is a low-potential power supply line.

12. A bias voltage generation circuit according to any one of the preceding claims, wherein said bias voltage (Vcs) generated by said bias voltage generation circuit is supplied to an emitter coupled logic circuit during said operation period (t_0).

Fig. 1

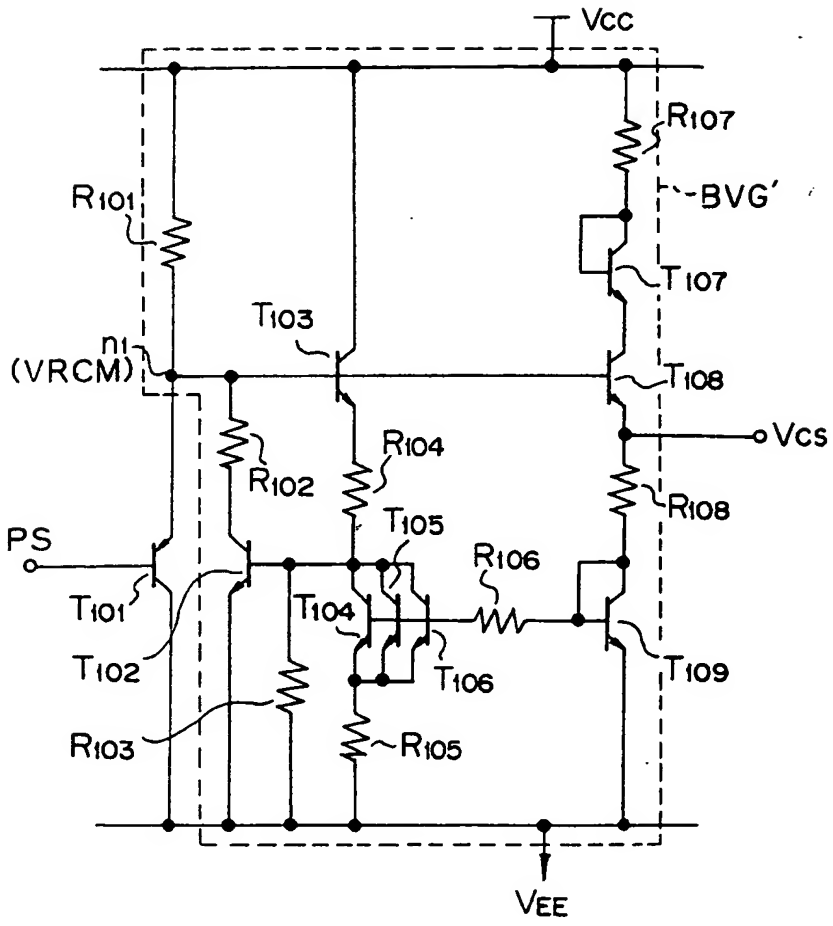

Vcc
R107
BVG'
R101
T107
T103
n1
(VRCM)
T108
Vcs
R104
R102
R108
T105
PS
R106
T101
T104
T102
T109
T106
R103
R105
VEE

Fig. 2

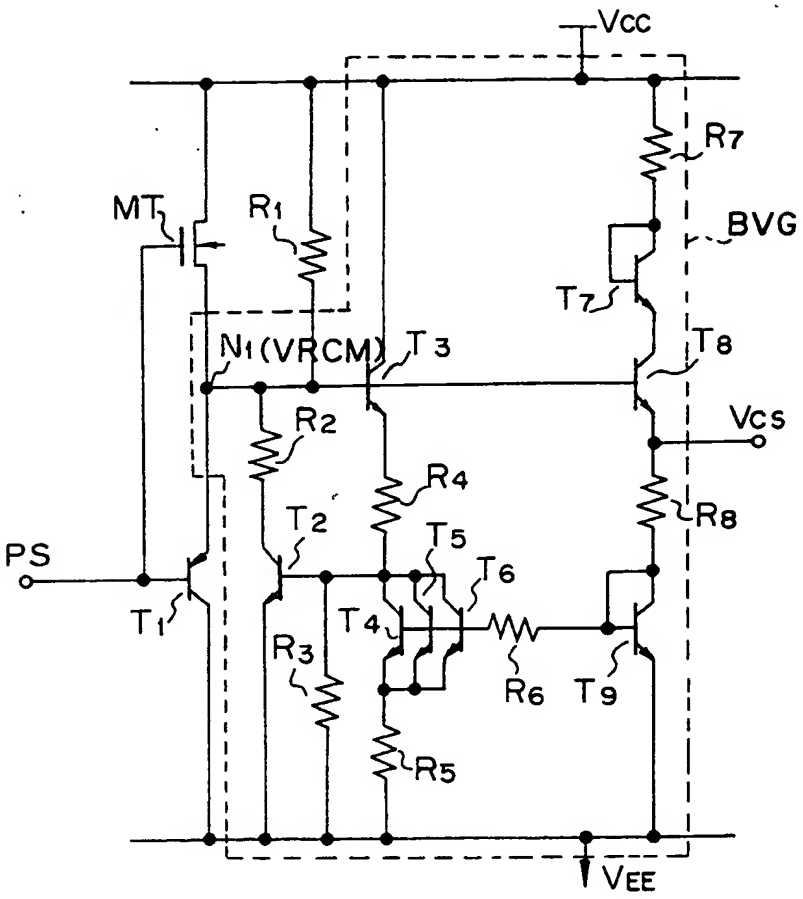

Vcc
R7
BVG
MT
R1
T7
N1(VRCM)
T3
T8
R2
Vcs
R4
R8
T2
T5
PS
T6
T1
T4
R3
R6
T9
R5
VEE

Fig. 3

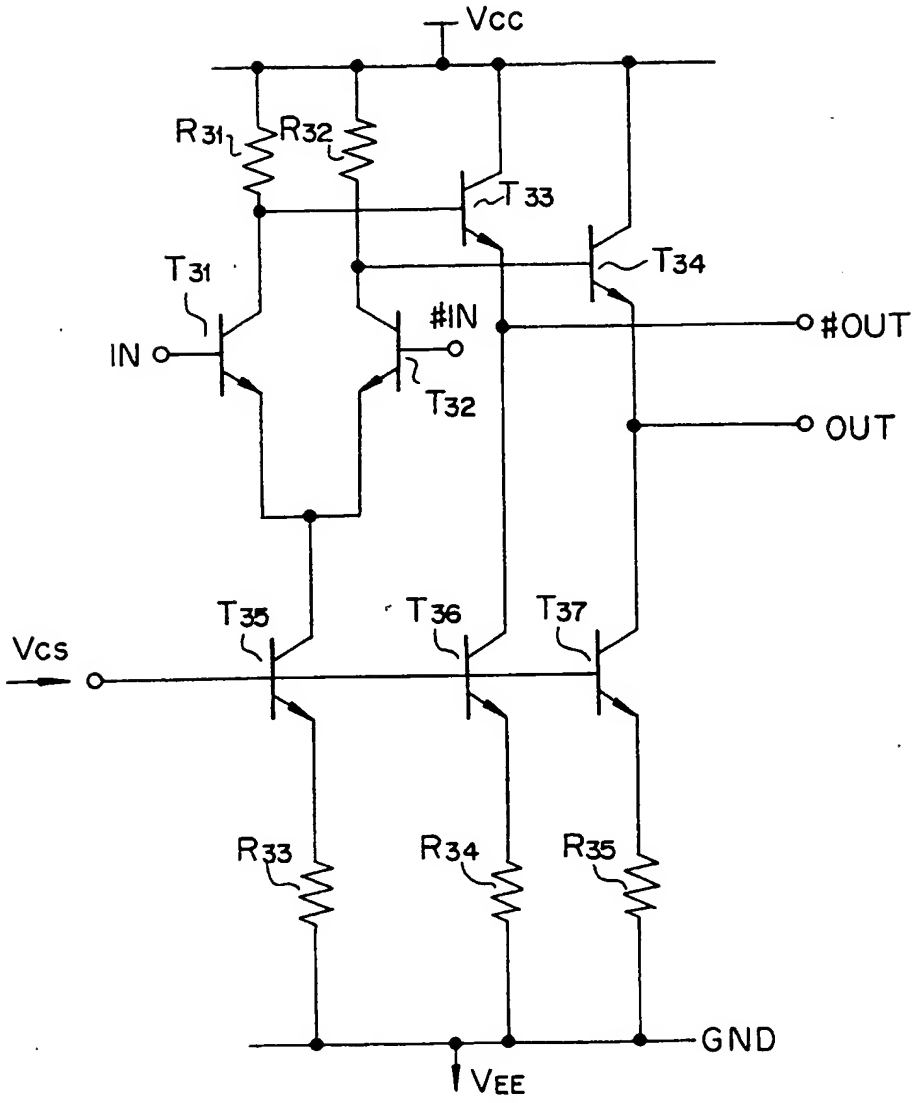

Vcc
R31
R32
T33
T34
T31
#IN
#OUT
IN
T32
OUT
T35
T36
T37
Vcs
R33
R34
R35
GND
VEE

Fig. 4

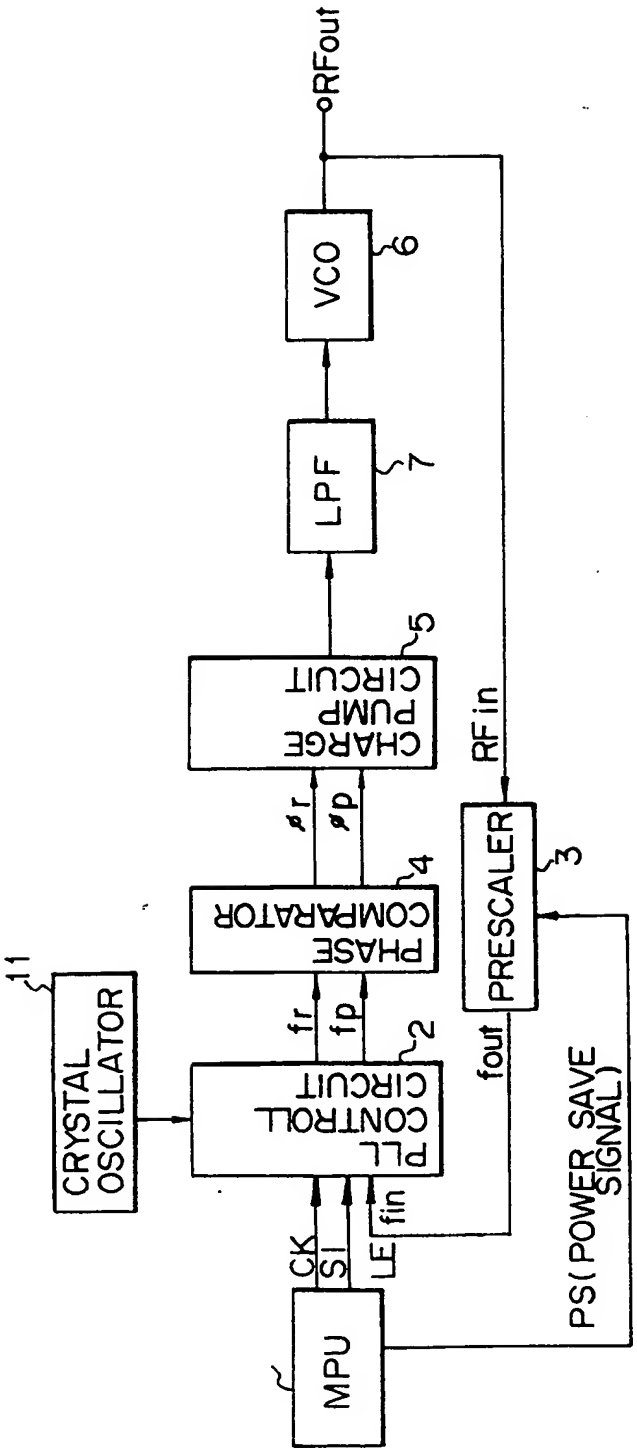
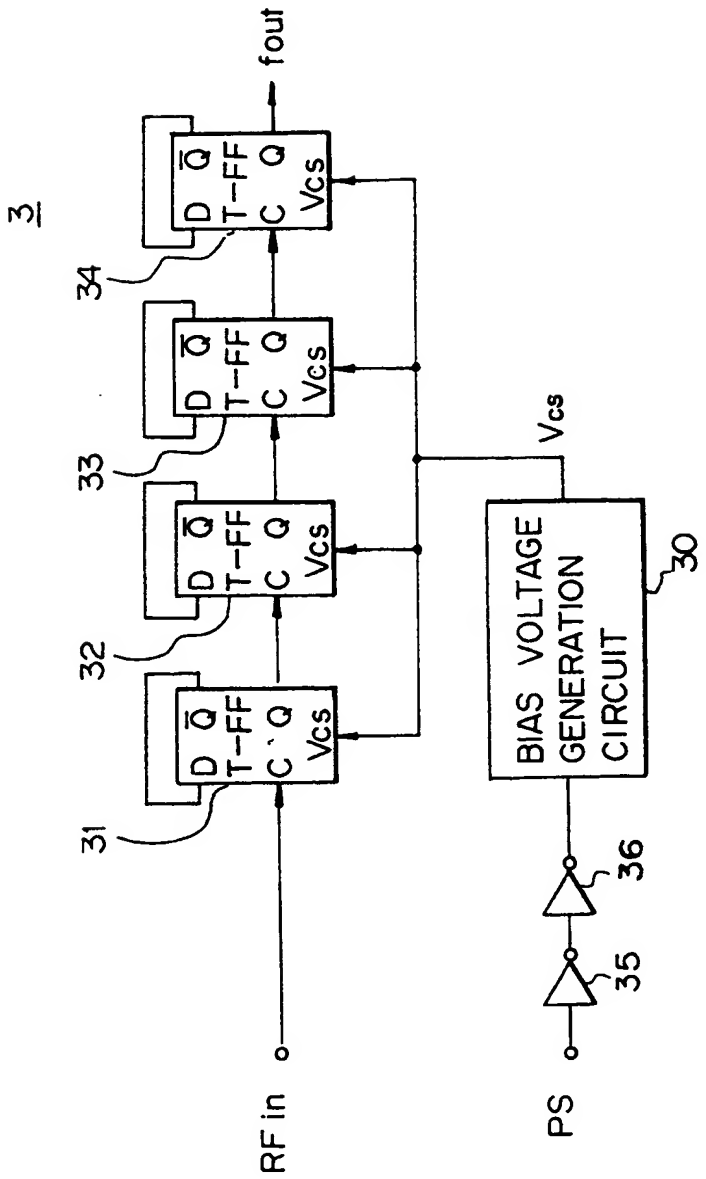

RFout
VCO
6
LPF
7
CHARGE PUMP CIRCUIT
5
RF in
PRESCALER
3
φr
φp
PHASE COMPARATOR
4
fout
PS(POWER SAVE SIGNAL)
11
CRYSTAL OSCILLATOR
fr
fp
PLL CONTROL CIRCUIT
2
fin
CK
SI
LE
MPU

Fig. 5


3
fout
D Q̄ T-FF C Q Vcs
34
33
32
31
Vcs
BIAS VOLTAGE GENERATION CIRCUIT
30
36
35
RF in
PS

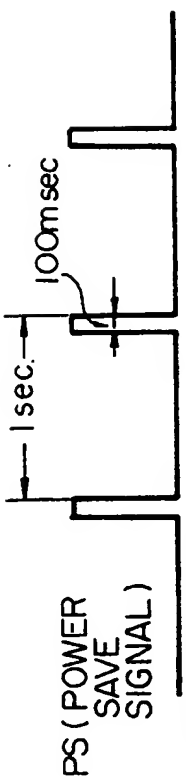


Fig. 6A

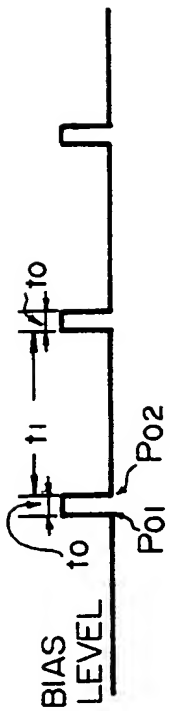


Fig. 6B

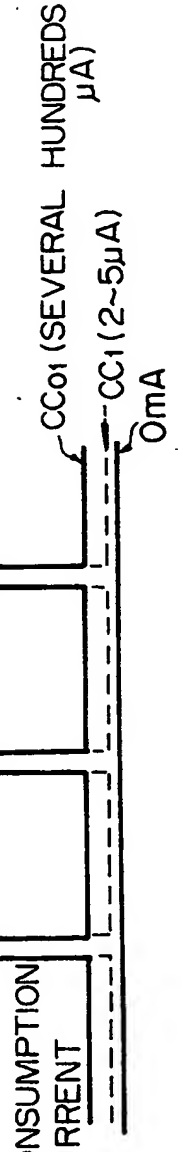


Fig. 6C

Fig. 7

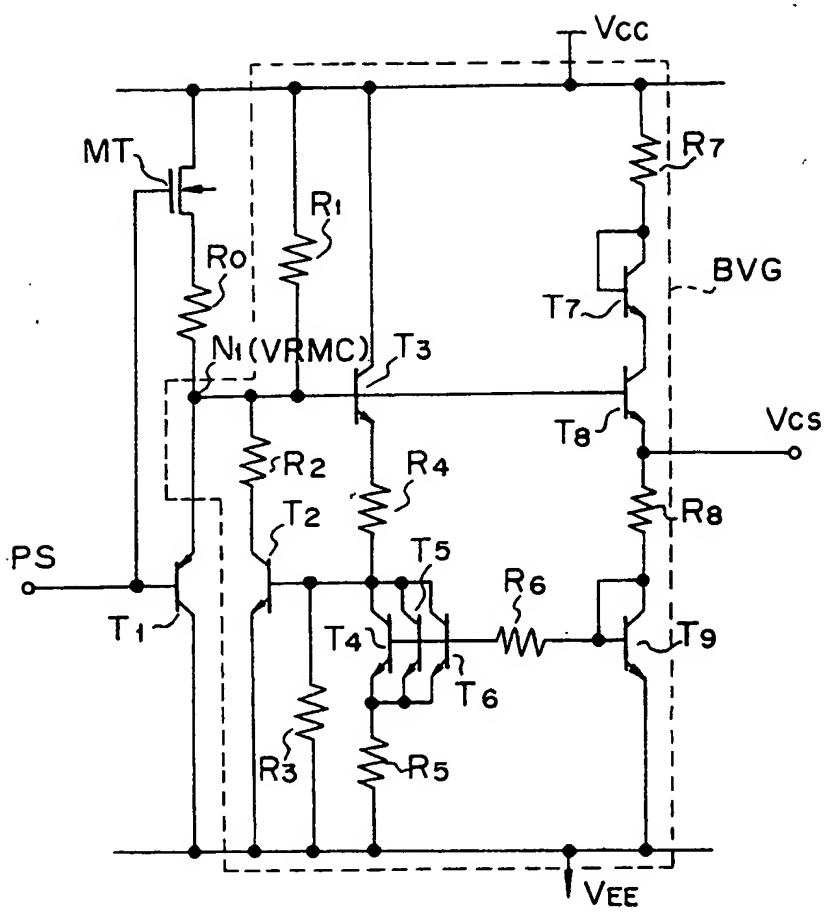
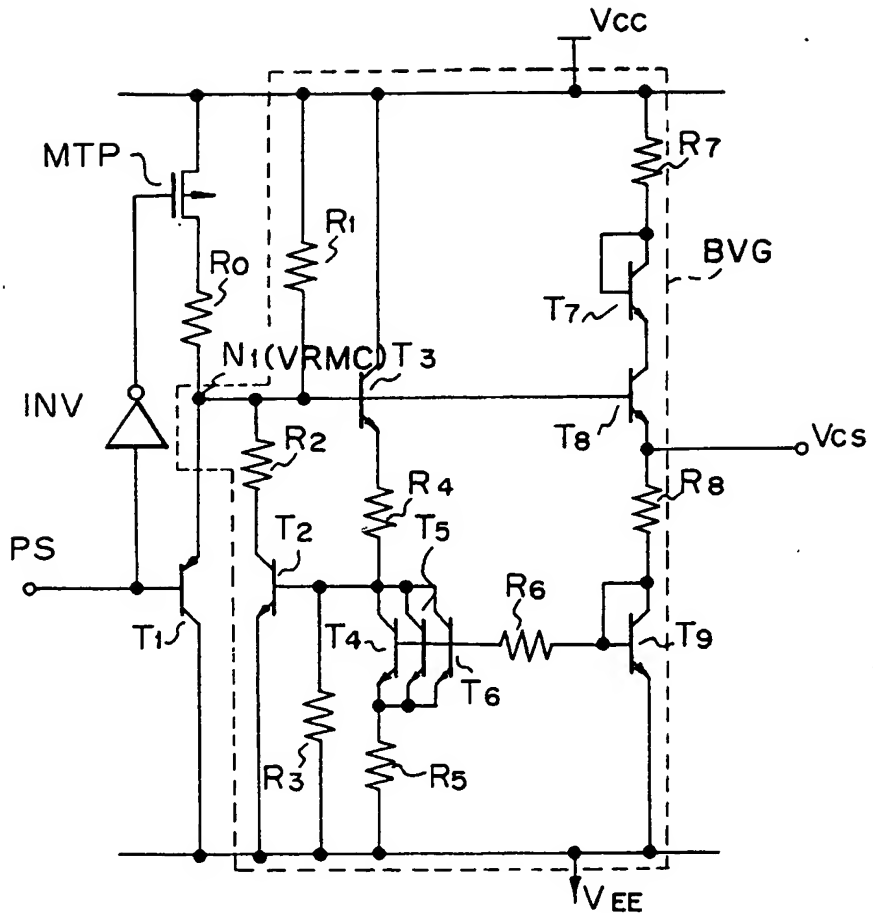

Vcc
MT
R1
R0
R7
BVG
T7
N1(VRMC)
T3
T8
Vcs
R2
R4
R8
T2
PS
T5
R6
T1
T4
T9
T6
R3
R5
VEE

Fig. 8


Vcc
MTP
R1
R0
R7
BVG
T7
N1(VRMC)
T3
INV
R2
T8
Vcs
R4
R8
PS
T2
T5
R6
T1
T4
T9
T6
R3
R5
VEE

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 30 2017

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 51 (P-667)(2898), 16 February 1988; & JP - A - 62197987 (MITSUBISHI ELECTRIC CORP) 01.09.1987	1,10-12	H 03 K 19/00 G 05 F 3/22
A	US-A-4 639 661 (B.J. WILLIAMS et al.) * whole document *	1	
A	EP-A-0 157 905 (KABUSHIKI KAISHA TOSHIBA) * whole document *	1	
A	IBM TECHNICAL DISCLOSURE BULLETIN vol. 29, no. 4, September 1986, pages 1780-1782; "Standby Circuit for Power Savings" * whole document *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 05 F 3/22
G 06 F 1/32
G 11 C 11/413
H 03 K 19/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	26-06-1992	ARENDT M

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